CLAIMS

What is claimed is:

1. A method, comprising:

reading a status of a buffer used to receive network packets transmitted from a different chip; and

transmitting to said different chip an unscheduled flow control packet including information about the status of the buffer.

2. The method of claim 1, wherein the buffer is associated with a port through which the network packets travel.

3. The method of claim 1, wherein the buffer is associated with an aggregate of ports through which different ones of the network packets travel.

4. The method of claim 1, wherein the network packets are Internet protocol ("IP") packets.

5. The method of claim 1, wherein each network packet is associated with a port through which the network packet will travel.

6. A method, comprising:

receiving a network packet from a sender chip, wherein the network packet was transmitted during a first period;

storing the network packet in a packet buffer, wherein the packet buffer is associated with a port through which the network packet will travel;

generating an unscheduled flow control packet, wherein the unscheduled flow control packet comprises information relating to the packet buffer; and

transmitting the unscheduled flow control packet to the sender chip, wherein the unscheduled flow control packet is transmitted during a second period, and wherein the second period is shorter than the first period.

7. The method of claim 6, wherein the unscheduled flow control packet comprises control data and port data.

8. The method of claim 7, wherein the port data comprises a bit pattern that is associated with the packet buffer being used in the aggregate.

9. The method of claim 7, wherein the control data requires one clock cycle for transmission during the second period, and wherein the port data requires four clock cycles for transmission during the second period.

10. The method of claim 7, wherein the control data includes a command from the Optical Internetworking Forum SPI-4 Phase 2 Implementation Agreement.

11. A method comprising:

periodically receiving network packets from a sender chip;

storing the network packets in a packet buffer; and

periodically transmitting flow control data back to the sender chip based on a status of the packet buffer and without regard to a calendar, wherein the flow control data comprises information relating to the packet buffer, and wherein each of said periodic transmissions of flow control data is faster than transmission of one of said network packets.

12. The method of claim 11, wherein the packet buffer is associated with a port through which the network packets travel.

13. The method of claim 11, wherein the packet buffer is associated with an aggregate of ports through which different ones of the network packets travel.

14. The method of claim 11, wherein the network packets are Internet protocol ("IP") packets.

15. The method of claim 11, wherein each network packet is associated with a port through which the network packet will travel.

16. A method, comprising:

receiving an unscheduled flow control packet from a different chip; and

modifying a rate at which a network packet is transmitted to said different chip, based on information in the unscheduled flow control packet.

17. The method of claim 16, wherein the recipient unit includes a buffer, wherein the unscheduled flow control packet comprises control data and port data, and wherein the unscheduled flow control packet is associated with the buffer.

18. The method of claim 17, wherein the buffer is associated with an aggregate of ports through which different ones of the network packets travel, and wherein the port data comprises a bit pattern that that is associated with the buffer being used in the aggregate among all available ports.

19. The method of claim 17, wherein the buffer is associated with a port through which the network packet will travel, and wherein the port data comprises a bit pattern that corresponds to the address of the port.

20. The method of claim 17, wherein the control data includes a command from the Optical Internetworking Forum SPI-4 Phase 2 Implementation Agreement.

21. A method, comprising:

receiving an unscheduled flow control packet from a recipient chip during a second period, wherein the second period is shorter than a first period during which a network packet is transmitted to the recipient chip, wherein the unscheduled flow control packet comprises information relating to a packet buffer within the recipient chip, and wherein the packet buffer is associated with a port; and

modifying a rate at which network packets are transmitted to the recipient chip based on the information in the unscheduled flow control packet.

22. The method of claim 21, wherein the unscheduled flow control packet comprises control data and port data.

23. The method of claim 22, wherein the port data comprises a bit pattern that that is associated with the packet buffer being used in the aggregate among all available ports.

24. The method of claim 23, wherein the port data comprises a bit pattern that corresponds to the address of the port.

25. The method of claim 23, wherein the control data requires one clock cycle for transmission during the second period, and wherein the port data requires four clock cycles for transmission during the second period.

26. The method of claim 23, wherein the control data includes a command from the Optical Internetworking Forum SPI-4 Phase 2 Implementation Agreement.

27. A chip, comprising:

a packet buffer to store network packets transmitted from a different chip, wherein the packet buffer is associated with one or more of a plurality of ports through which the network packets travel; and

control circuitry, coupled with a packet data bus to receive said network packets from the different chip, and coupled with an unscheduled flow control packet bus to generate and transmit unscheduled flow control packets to the different chip, wherein the unscheduled flow control packets contain information relating to the packet buffer.

28. The chip of claim 27, wherein the unscheduled flow control packet comprises control data and port data.

29. The chip of claim 28, wherein the packet buffer is associated with all of the plurality of ports, and wherein the port data comprises a bit pattern that is associated with the packet buffer being used in the aggregate among all available ports.

30. The chip of claim 29, wherein the packet buffer is associated with one of the plurality of ports , and wherein the port data comprises a bit pattern that corresponds to the address of the port.

31. A chip, comprising:

flow control logic, coupled with an unscheduled flow control packet bus to receive an unscheduled flow control packet from a different chip; and

network packet logic, coupled with a packet data bus and the flow control logic, to modify, in response to the unscheduled flow control packet, a rate at which network packets are transmitted to the different chip, wherein each of the network packets is associated with one of a plurality of ports through which that network packet will travel.

32. The chip of claim 31, wherein the different chip includes a buffer, wherein the unscheduled flow control packet comprises control data and port data, and wherein the unscheduled flow control packet is associated with the buffer.

33. The chip of claim 32, wherein the buffer is associated with all of the plurality of ports, and wherein the port data comprises a bit pattern that that is associated with the buffer being used in the aggregate among all available ports.

34. The chip of claim 32, wherein the buffer is associated with one of the plurality of ports through which the network packet will travel, and wherein the port data comprises a bit pattern that corresponds to the address of the port.

35. The chip of claim 32, wherein the control data includes a command from the Optical Internetworking Forum SPI-4 Phase 2 Implementation Agreement.